Q.P. Code: 16EC408 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Regular & Supplementary Examinations May 2019

COMPUTER ORGANIZAION & ARCHITECTURE

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Differentiate high level and low level languages.	4M
	b	Design an 8x4 memory subsystem constructed from two 8x2 ROM chips?	4M
	c	Justify importance of backward compatibility in processor design with practical examples.	4M
		OR	
2	**a**	With suitable paradigms, describe the instruction types used in Assembly level languages.	7M
	b	Elaborate how CPU is concordant with its input & output devices and explain the interfacing modules involved?	5M
		UNIT-II	
3	**a**	Write about interrupt and its types?	6M
	b	With a neat schematic, explain the steps involved in fetch and decode phases using register transfer instructions.	6M
		OR	
4	**a**	Explain in detail about booth multiplication algorithm with an example	8M
	b	What is an instruction cycle and write the phases of instruction cycle.	4M
		UNIT-III	
5	**a**	Differentiate Hardwired and Micro programmed control unit. Is it possible to have a hardwired control associated with a control memory?	4M
	b	Design and implement 4-bit arithmetic unit which performs ADD, ADD with carry, SUB, Sub with borrow, increment and decrement operations.	8M
		OR	
6	**a**	Implement bus line for an 8-bit register using three state-buffers.	6M
	b	Explain about address sequencing in control memory with neat diagrams.	6M
		UNIT-IV	
7		Classify and describe the possible modes of data transfer to and from peripherals with examples.	12M
		OR	
8	**a**	What is the disadvantage of strobe method and explain how handshake method solves the problem?	6M
	b	What is virtual memory? Explain the relation between address space and memory space in a virtual memory system along with its memory table for mapping.	6M
		UNIT-V	
9	**a**	Classify organization of computers using Flynn's criteria.	4M
	b	Explain in detail about crossbar switching, multistage switching network and hypercube system.	8M
		OR	
10	**a**	Write about Time shared common bus and multiport memory.	8M
	b	A non-pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock of 10 ns. Determine speedup ratio of the pipeline for 100 tasks.	4M

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